CLAIMS

What is claimed is:

1. A method for modifying stress formation in a semiconductor structure comprising the steps of:

providing a structure having a patterned material stack located on top of a surface of a semiconductor substrate, said patterned material stack having at least one opening that exposes a portion of the semiconductor substrate;

forming at least one trench into the exposed portion of the semiconductor substrate, each trench having sidewalls that extend to a common bottom wall; and

subjecting at least one of the sidewalls of each trench and a portion of the common bottom wall of each trench to a plasma nitridation process.

2. The method of Claim 1 wherein the plasma nitridation process is performed prior to filling the at least one trench with a trench dielectric.

3. The method of Claim 1 wherein the plasma nitridation process is performed after filling the at least one trench with a trench dielectric.

4. The method of Claim 3 wherein, prior to performing the plasma nitridation process and after filling, preselected portions of the patterned material stack are removed and a block mask is formed over active areas of the semiconductor substrate in which PFETs are to be formed.

5. The method of Claim 4 wherein the block mask comprises an edge portion that extends beyond one sidewall of the at least one trench.

6. The method of Claim 1 wherein the patterned material stack comprises at least a bottom pad oxide and a top pad nitride.

7. The method of Claim 1 wherein the plasma nitridation process is carried out at in a nitrogen-containing atmosphere.

8. The method of Claim 7 wherein the nitrogen-containing atmosphere comprises N_2, NO, N_2O, NH_3 and mixtures thereof.

9. The method of Claim 7 wherein the nitrogen-containing atmosphere is admixed with an inert gas selected from the group consisting of He, Ar, Ne, Kr, Xe and mixtures thereof.

10. The method of Claim 1 wherein the plasma nitridation process comprises a plasma of N_2 in He.

11. The method of Claim 1 wherein the plasma nitridation process is carried out using a plasma having a temperature of about 80°C or below, while maintaining the substrate at a temperature of from about 20° C to about 100°C.

12. The method of Claim 10 wherein the plasma nitridation process comprises a rapid thermal nitridation process in which the nitridation is performed for about 120 seconds or less.

13. The method of Claim 1 wherein the plasma nitridation process is a decoupled plasma nitridation (DPN) process.

14. The method of Claim 13 wherein the DPN process is performed using 2-10% N_2 in He at a pressure range between 50-100 mTorr, a power range from 50-200 Watts, and a plasma exposure time of from: 10-50 seconds.

15. A semiconductor structure comprising

a semiconductor substrate having at least one trench isolation region located therein, said at least one trench isolation region having sidewalls that extend to a common bottom wall; and

a nitride liner present at least on portions of the sidewalls, said nitride liner protecting the sidewalls of the at least one trench so as to reduce stress in the semiconductor substrate.

16. The semiconductor structure of Claim 15 wherein the nitride liner is present on the entire sidewalls and bottom wall of the at least one trench.

17. The semiconductor structure of Claim 15 wherein the nitride liner is a nitrided surface layer that has a thickness of about 0.1 to about 2.0 nm.

18. The semiconductor structure of Claim 15 further comprising NFET device regions and PFET device regions.

19. The semiconductor structure of Claim 18 wherein the trenches adjoining the NFETs contain the nitride liner on the entire sidewalls and bottom wall of each trench.

20. The semiconductor structure of Claim 18 wherein the sidewalls of the trenches adjoining the PFETs are void of any nitride liner.